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REMARKS

The Applicants appreciate the thorough examination of the present application as evidenced by the Official Action mailed May 17, 2004 (hereinafter "the Official Action"). In particular, the Applicants appreciate the Examiner's indication that Claims 14, 18, and 19 would be allowable if rewritten in independent form. The Applicants also appreciate the Examiner's indication that Claim 30 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. Sec. 112, second paragraph, and if rewritten in independent form.

In response to the Official Action, the Applicants have amended Claims 2, 11, 20, and 32 to overcome minor informalities noted by the Examiner. The Applicants have not, however, rewritten Claims 14, 18, 19, and 30 in independent form, because the Applicants will show in the following remarks that Independent Claims 1 and 20 are patentable over the cited art. The Applicants thus submit that all claims are in condition for allowance as discussed in greater detail below.

All Rejections Under 35 U.S.C. Sec. 112 Have Been Overcome

Claims 2, 11, and 20-32 have been rejected under 35 U.S.C. Sec. 112, second paragraph. In response, the Applicants have amended Claims 2, 11, 20, and 32 as requested by the Examiner. The Applicants thus submit that all rejections under 35 U.S.C. Sec. 112 have been overcome. The Applicants further submit that the amendments of Claims 2, 11, 20, and 32 relate to the correction of minor informalities, and that these amendments have not been made to address art rejections. Accordingly, the amendments of Claims 2, 11, 20, and 32 do not narrow the scope of these claims.

Independent Claim 1 Is Patentable

Independent Claim 1 has been rejected under 35 U.S.C. Sec. 102(e) as being anticipated by U.S. Patent Publication No. 2003/0038323 to Kotani. The Applicants respectfully submit, however, that Claim 1 is patentable for at least the reasons discussed below.

More particularly, Claim 1 recites a method of forming an electronic device. The method of Claim 1 includes:

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forming a capacitor structure on a portion of a substrate, the capacitor structure including a first electrode on the substrate, a capacitor dielectric on the first electrode, a second electrode on the dielectric, and a hard mask on the second electrode so that the capacitor dielectric is between the first and second electrodes, so that the first electrode and the capacitor dielectric are between the second electrode and the substrate, and so that the first and second electrodes and the capacitor dielectric are between the hard mask and the substrate:

forming an interlayer dielectric layer on the hard mask and on portions of the substrate surrounding the capacitor structure;

removing portions of the interlayer dielectric layer to expose the hard mask while maintaining portions of the interlayer dielectric layer on portions of the substrate surrounding the capacitor structure; and

removing the hard mask thereby exposing portions of the second electrode while maintaining the portions of the interlayer dielectric layer on portions of the substrate surrounding the capacitor.

In presenting the rejection of Claim 1, the Office Action states that:

Kotani discloses forming a semiconductor element 2, which could be a capacitor structure on a portion of a substrate 50 including forming a first electrode on the substrate, forming a capacitor dielectric on the first electrode, forming a second electrode on the dielectric, and forming a hard mask 4 on the second electrode (Figure 7, and Paragraphs 0046, and 0094)....

Office Action, pages 2-3. Moreover, Kotani states that:

Although the semiconductor elements formed in the Si layer 2 have been field-effect transistors in the foregoing embodiment, the present invention can also use other semiconductor elements such as capacitor elements, resistor elements, and diodes.

Kotani, paragraph 0094.

The Applicants respectfully submit, however, that to anticipate a claim, the reference must teach every element of the claim. As set forth in the Manual Of Patent Examining Procedure (MPEP):

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegall Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

MPEP, Sec. 2131.

Kotani does not teach or suggest that the semiconductor element 2 is a capacitor, or that a capacitor including first and second electrodes and a capacitor dielectric could be substituted for the semiconductor element 2. With respect to the

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illustrated embodiments of Kotani, the semiconductor element 2 is not a complete transistor. Instead, the semiconductor element 2 provides an active region of a transistor, and gate oxide film 28 and the gate electrode 29 are provided on the semiconductor element 2 after removing the mask 4. (*See*, Kotani, page 5, paragraphs 0073-0075.) While Kotani states that "the invention can use other semiconductor elements such as capacitor elements...", Kotani does not teach or suggest substituting a complete capacitor including first and second electrodes and a capacitor dielectric for the semiconductor element 2. Moreover, such a substitution would be contrary to the teachings of Kotani.

Applicants believe that paragraph 0094 should be interpreted to mean that the semiconductor element 2 could be used as an element of a capacitor with other elements of the capacitor being formed after removing the mask 4. This interpretation is consistent with the discussion of the illustrated embodiments where the semiconductor element 2 provides an active region of a transistor, and gate oxide film 28 and gate electrode 29 of the transistor are formed after removing the mask 4. Accordingly, Kotani fails to teach or suggest a capacitor structure including first and second electrodes, a capacitor dielectric between the first and second electrodes, and a hard mask on the second electrode. The Applicants thus submit that Claim 1 is patentable over Kotani. The Applicants further submit that Dependent Claims 2-19 are patentable at least as per the patentability of Claim 1 from which they depend. In addition, Dependent Claims 14, 18, and 19 have also been indicated in the Official Action as being independently patentable.

Independent Claim 20 Is Patentable

Claim 20 has been rejected under 35 U.S.C. Sec. 103(a) as being unpatentable over Kotani in view of U.S. Patent No. 6,020,233 to Kim and U.S. Patent No. 6,376,325 to Koo. The Applicants respectfully submit that Claim 20 is patentable over the cited art.

In particular, Claim 20 recites a method of fabricating a ferroelectric memory device. This method includes:

forming a lower interlayer dielectric on a semiconductor substrate; sequentially stacking a ferroelectric capacitor and a hard mask pattern on the lower interlayer dielectric;

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forming an inter-metal dielectric to cover an entire surface of the semiconductor substrate including the hard mask pattern;

planarizing the inter-metal dielectric to expose the hard mask pattern; selectively removing the exposed hard mask pattern to expose a top surface of the ferroelectric capacitor; and

forming a plate line contacting with the top surface of the ferroelectric capacitor.

As discussed above, Kotani fails to teach or suggest a capacitor structure including first and second electrodes, a capacitor dielectric between the first and second electrodes, and a hard mask on the second electrode. Accordingly, Kotani fails to teach or suggest sequentially stacking a ferroelectric capacitor and a hard mask pattern on a lower interlayer dielectric. Moreover, neither Kim and/or Koo provides these missing teachings, and the Office Action does not point to portions or either Kim and/or Koo as providing these missing teachings.

Accordingly, the Applicants respectfully submit that the combination of Kotani, Kim, and Koo fails to teach or suggest the method of Claim 20 and that Claim 20 is thus patentable. Moreover, Dependent Claims 21-33 are patentable at least as per the patentability of Claim 20 from which they depend. In addition, Dependent Claim 30 has also been indicated in the Official Action as being independently patentable.

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CONCLUSION

Accordingly, the Applicants submit that all pending claims in the present application are in condition for allowance, and allowance of all claims is respectfully requested in due course. The Examiner is encouraged to contact the undersigned attorney by telephone if any additional issues should need to be addressed.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on August 6, 2004.

Joyce Paoli